What is claimed is:

1. An NROM memory transistor comprising:
a substrate having a plurality of source/drain regions, the source/drain regions having a different conductivity type than the remainder of the substrate;
a nanolaminate gate dielectric formed on top of the substrate substantially between the plurality of source/drain regions, the gate dielectric having a dielectric constant greater than silicon dioxide; and
a control gate formed on top of the gate dielectric.

2. The transistor of claim 1 wherein the gate dielectric is a composite oxide – high-k dielectric – oxide nanolaminate gate insulator wherein the high-k dielectric is a charge trapping layer.

3. The transistor of claim 2 wherein the charge trapping layer is comprised of a material that has a lower conduction band edge than silicon nitride.

4. The transistor of claim 2 wherein the gate dielectric has a larger energy barrier between the high-k dielectric and the oxide insulator than silicon dioxide.

5. The transistor of claim 1 wherein the gate dielectric is comprised of one of the following structures: oxide – atomic layer deposited (ALD) $HfO_2$ – oxide, oxide – evaporated $HfO_2$ – oxide, oxide – ALD $ZrO_2$ – oxide, oxide – evaporated $ZrO_2$ – oxide, oxide – ALD ZrSnTiO – oxide, oxide – ALD ZrON – oxide, oxide – evaporated ZrON – oxide, oxide – ALD ZrAlO – oxide, oxide – ALD $ZrTiO_4$ – oxide, oxide – ALD $Al_2O_3$ – oxide, oxide – ALD $La_2O_3$ – oxide, oxide – ALD $LaAlO_3$ – oxide, oxide – evaporated $LaAlO_3$ – oxide, oxide – ALD $HfAlO_3$ – oxide, oxide – ALD HfSiON – oxide, oxide – evaporated $Y_2O_3$ – oxide, oxide – evaporated $Gd_2O$ – oxide, oxide – ALD $Ta_2O_5$ – oxide, oxide – ALD $TiO_2$ – oxide, oxide – evaporated $TiO_2$ – oxide, oxide – ALD $Pr_2O_3$ – oxide, oxide – evaporated

$Pr_2O_3$ – oxide, oxide – evaporated $CrTiO_3$ – oxide, or oxide – evaporated YSiO – oxide.

6. An NROM memory transistor comprising:
a substrate having a plurality of source/drain regions, the source/drain regions having a different conductivity than the remainder of the substrate;
a composite gate insulator layer formed on top of the substrate and substantially between the plurality of source/drain regions, the gate insulator comprises a trapping layer having a higher dielectric constant than silicon dioxide; and
a control gate formed on top of the gate insulator layer.

7. The transistor of claim 6 wherein the composite gate insulator comprises an oxide – nitride – high-k dielectric structure.

8. The transistor of claim 6 wherein the plurality of source/drain regions are comprised of an n+ type doped silicon.

9. The transistor of claim 6 wherein the control gate is a polysilicon material.

10. The transistor of claim 6 wherein the substrate is comprised of a p+ type silicon material.

11. The transistor of claim 6 wherein the composite gate insulator layer is comprised of one of the following structures: oxide – nitride – atomic layer deposited (ALD) $Al_2O_3$, oxide – nitride – ALD $HfO_2$, or oxide – nitride – ALD $ZrO_2$.

12. An NROM memory transistor comprising:
a substrate having a plurality of source/drain regions, the source/drain regions having a different conductivity than the remainder of the substrate;

a composite gate insulator layer formed on top of the substrate and substantially between the plurality of source/drain regions, the gate insulator comprises a structure having a plurality of layers each having a dielectric constant that is higher than silicon dioxide; and

a control gate formed on top of the gate insulator layer.

13. The transistor of claim 12 wherein the substrate is comprised of a p+ type conductivity silicon and the source/drain regions are n+ doped regions in the substrate.

14. The transistor of claim 12 wherein the composite gate insulator layer is comprised of one of the following structures: atomic layer deposited (ALD) $HfO_2$ – ALD $Ta_2O_5$ – ALD $HfO_2$, ALD $La_2O_3$ – ALD $HfO_2$ – ALD $La_2O_3$, ALD $HfO_2$ – ALD $ZrO_2$ – ALD $HfO_2$, ALD Lanthanide (Pr, Ne, Sm, Gd, and Dy) Oxide – ALD $ZrO_2$ – ALD Lanthanide Oxide, ALD Lanthanide Oxide – ALD $HfO_2$ – ALD Lanthanide Oxide, or ALD Lanthanide Oxide – evaporated $HfO_2$ – ALD Lanthanide Oxide.

15. An electronic system comprising:

a processor that generates control signals; and

a memory array coupled to the processor, the array comprising a plurality of NROM memory cells, each NROM memory cell comprising:

a substrate having a plurality of source/drain regions, the source/drain regions having a different conductivity than the remainder of the substrate;

a nanolaminate gate dielectric formed on top of the substrate substantially between each pair of the plurality of source/drain regions, the gate dielectric having a dielectric constant greater than silicon dioxide; and

a control gate formed on top of the oxide insulator.

16. A method for fabricating an NROM memory cell, the method comprising:
creating a plurality of source/drain regions by doping portions of a substrate;
forming a nanolaminate gate dielectric layer on the substrate substantially between the plurality of source/drain regions, the gate dielectric layer having a dielectric constant that is higher than silicon dioxide; and
forming a control gate on the oxide insulator material.

17. The method of claim 16 wherein the plurality of source/drain regions are created with a p+ conductivity in an n+ substrate.

18. The method of claim 16 wherein the gate dielectric layer is comprised of an oxide – high-k dielectric – oxide structure.

19. The method of claim 16 wherein the gate dielectric layer is comprised of an oxide – nitride – high-k dielectric structure.

20. The method of claim 16 wherein the gate dielectric layer is comprised of a high-k dielectric – high-k dielectric – high-k dielectric structure.

21. The method of claim 16 wherein forming the gate dielectric layer comprises forming one of the following structures: oxide – atomic layer deposited (ALD) $HfO_2$ – oxide, oxide – evaporated $HfO_2$ – oxide, oxide – ALD $ZrO_2$ – oxide, oxide – evaporated $ZrO_2$ – oxide, oxide – ALD ZrSnTiO – oxide, oxide – ALD ZrON – oxide, oxide – evaporated ZrON – oxide, oxide – ALD ZrAlO – oxide, oxide – ALD $ZrTiO_4$ – oxide, oxide – ALD $Al_2O_3$ – oxide, oxide – ALD $La_2O_3$ – oxide, oxide – ALD $LaAlO_3$ – oxide, oxide – evaporated $LaAlO_3$ – oxide, oxide – ALD $HfAlO_3$ – oxide, oxide – ALD HfSiON – oxide, oxide – evaporated $Y_2O_3$ – oxide, oxide – evaporated $Gd_2O$ – oxide, oxide – ALD $Ta_2O_5$ – oxide, oxide – ALD $TiO_2$ – oxide, oxide – evaporated $TiO_2$ – oxide, oxide – ALD $Pr_2O_3$ – oxide, oxide –

evaporated $Pr_2O_3$ – oxide, oxide – evaporated $CrTiO_3$ – oxide, or oxide – evaporated YSiO – oxide.

22. The method of claim 16 wherein forming the gate dielectric layer comprises forming one of the following structures: oxide – nitride – atomic layer deposited (ALD) $Al_2O_3$, oxide – nitride – ALD $HfO_2$, or oxide – nitride – ALD $ZrO_2$

23. The method of claim 16 wherein forming the gate dielectric layer comprises forming one of the following structures: atomic layer deposited (ALD) $HfO_2$ – ALD $Ta_2O_5$ – ALD $HfO_2$, ALD $La_2O_3$ – ALD $HfO_2$ – ALD $La_2O_3$, ALD $HfO_2$ – ALD $ZrO_2$ – ALD $HfO_2$, ALD Lanthanide (Pr, Ne, Sm, Gd, and Dy) Oxide – ALD $ZrO_2$ – ALD Lanthanide Oxide, ALD Lanthanide Oxide – ALD $HfO_2$ – ALD Lanthanide Oxide, or ALD Lanthanide Oxide – evaporated $HfO_2$ – ALD Lanthanide Oxide.

24. The method of claim 16 wherein forming the gate dielectric layer comprises an atomic layer deposition technique.

25. The method of claim 16 wherein forming the gate dielectric layer comprises an evaporation technique.

26. The method of claim 16 wherein forming the gate dielectric layer comprises an atomic layer deposition technique and an evaporation technique.

27. A method for fabricating an NROM memory cell, the method comprising:
creating a plurality of source/drain regions by doping portions of a substrate;
depositing a tunnel oxide layer on the substrate substantially between the plurality of source/drain regions;

depositing a gate dielectric layer with an evaporation technique on the tunnel oxide layer, the gate dielectric layer having a dielectric constant that is higher than silicon dioxide;

depositing an oxide layer on the gate dielectric layer; and

forming a control gate on the oxide insulator material.

28. The method of claim 27 wherein depositing the gate dielectric layer comprises evaporating one of the following materials: $HfO_2$, ZrO2, ZrON, $LaAlO_3$, $Y_2O_3$, $Gd_2O$, $TiO_2$, $CrTiO_3$, or YSiO.

29. A method for fabricating an NROM memory cell, the method comprising:

creating a plurality of source/drain regions by doping portions of a substrate;

depositing a tunnel oxide layer on the substrate substantially between the plurality of source/drain regions;

depositing a gate dielectric layer with an atomic layer deposition technique on the tunnel oxide layer, the gate dielectric layer having a dielectric constant that is higher than silicon dioxide;

depositing an oxide layer on the gate dielectric layer; and

forming a control gate on the oxide insulator material.

30. The method of claim 29 wherein the gate dielectric layer comprises atomic layer deposition of one of the following materials: $HfO_2$, $ZrO_2$, ZrSnTiO, ZrON, ZrAlO, $ZrTiO_4$, $Al_2O_3$, $La_2O_3$, $LaAlO_3$, $HfAlO_3$, HfSiON, $Ta_2O_5$, $TiO_2$, or $Pr_2O_3$.

31. A method for fabricating an NROM memory cell, the method comprising:

creating a plurality of source/drain regions by doping portions of a substrate;

depositing a tunnel oxide layer on the substrate substantially between the plurality of source/drain regions;

depositing a nitride layer on the gate dielectric layer; and

depositing a gate dielectric layer with an atomic layer deposition technique on the nitride layer, the gate dielectric layer having a dielectric constant that is higher than silicon dioxide;

forming a control gate on the oxide insulator material.

32. The method of claim 31 wherein depositing the gate dielectric layer comprises atomic layer deposition of one of the following materials: $Al_2O_3$, $HfO_2$, or $ZrO_2$.

33. A method for fabricating an NROM memory cell, the method comprising:

creating a plurality of source/drain regions by doping portions of a substrate;

depositing a nanolaminate gate dielectric layer with an atomic layer deposition technique on the substrate substantially between the plurality of source/drain regions, the gate dielectric layer having a dielectric constant that is higher than silicon dioxide; and

forming a control gate on the oxide insulator material.

34. The method of claim 33 wherein depositing the nanolaminate gate dielectric layer comprises depositing one of the following nanolaminate structures: ALD $HfO_2$ – ALD $Ta_2O_5$ – ALD $HfO_2$, ALD $La_2O_3$ – ALD $HfO_2$ – ALD $La_2O_3$, ALD $HfO_2$ – ALD $ZrO_2$ – ALD $HfO_2$, ALD Lanthanide (Pr, Ne, Sm, Gd, and Dy) Oxide – ALD $ZrO_2$ – ALD Lanthanide Oxide, ALD Lanthanide Oxide – ALD $HfO_2$ – ALD Lanthanide Oxide, or ALD Lanthanide Oxide – evaporated $HfO_2$ – ALD Lanthanide Oxide.